Application Note No. 1

WALNUT 1-2400

DIGITAL DEVICES INC.

212 MICHAEL DRIVE • SYOSSET, LONG ISLAND, N. Y.

PROBLEM: Provide accurate delay of analog information for long periods of time with continuous recirculation including timing pulses to indicate start of information.

APPLICATIONS: Correlation studies, radar de-fruiting, temporary storage and recirculation for display, temporary storage to allow recording systems to accelerate to operating speed, storage for delayed digitizing and for slow speed recording of high-speed transient data.

30 Millisecond Analog Delay Line

SOLUTION: The accompanying photograph shows Digital's solution to the problem of precise analog delays. Timing information is superimposed on the same delay line as the data, using double amplitude for the timing pulse to ensure reliable separation.

Bandwidths of 1 mc with delays up to 15 msec are possible with a single line. Greater delays, of short duration information can be handled by "counting" timing pulses and gating the information out after an appropriate number of recirculations. Greater delays of information lasting longer than the basic line delay can be handled by using lines in tandem.

Analog information is first "digitized" by fm techniques and appropriate shaping so the fm crossovers appear as fast-rising logical changes at the input and output terminals of the system.

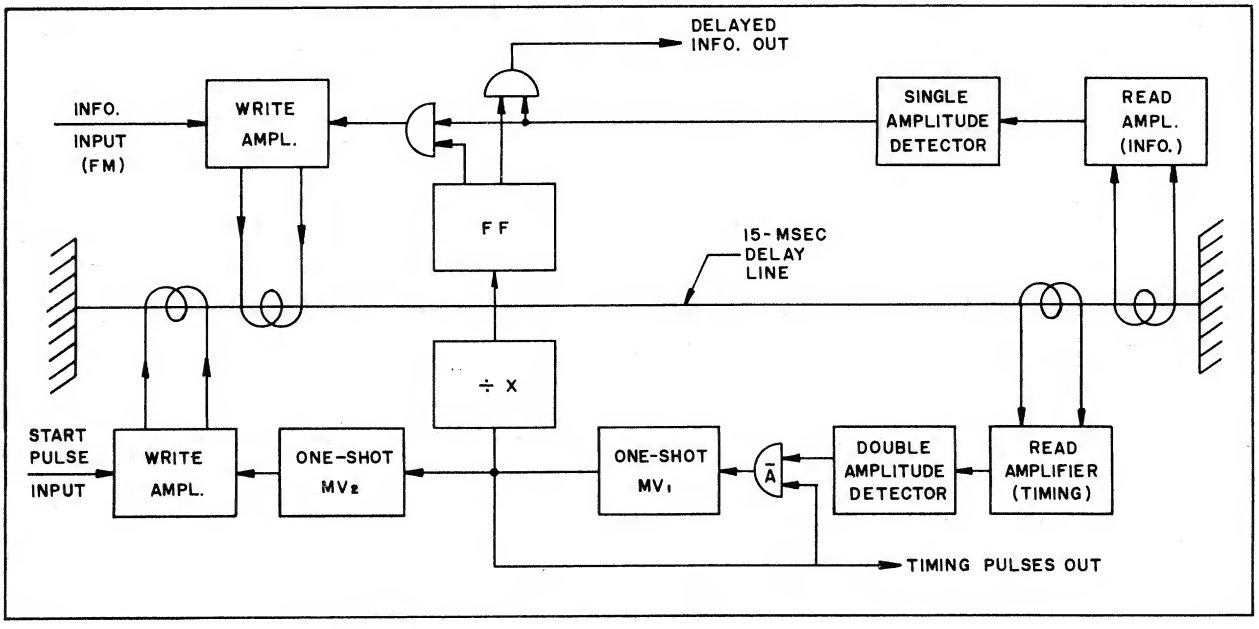
As illustrated in the photograph, read/write amplifiers and all necessary logic can be housed within the delay line case. A limited number of taps may be attached to the line for special timing purposes.

The block diagram below shows, in somewhat simplified form, the circuit components required. For simplicity, the separate sets of transducers are used, one for the information channel and one for timing. Timing pulses are of double amplitude so they can be distinguished from the information. In the standard system the single timing pulse is also accepted by the information detector, but it can be eliminated logically from the information output if required.

Multivibrator MV_1 is a one-shot circuit adjusted to remain <u>on</u> for almost the period of the line. Together with the <u>nand</u> gate, this excludes noise and any spurious pulses generated by the detector from being recirculated. If no start pulse is used, MV_1 is connected as an astable multivibrator and the system is self-starting and operates continuously.

Multivibrator MV_2 shapes the leading edge of MV_1's output for producing the double amplitude input through the timing channel write amplifier.

Divider X produces an output pulse after a predetermined number of timing pulses (recirculations) have been counted. This pulse sets the flip-flop and routes the information to the output terminal instead of the information channel write amplifier.



Application Note No. 2

WALNUT 1-2400

DIGITAL DEVICES INC.

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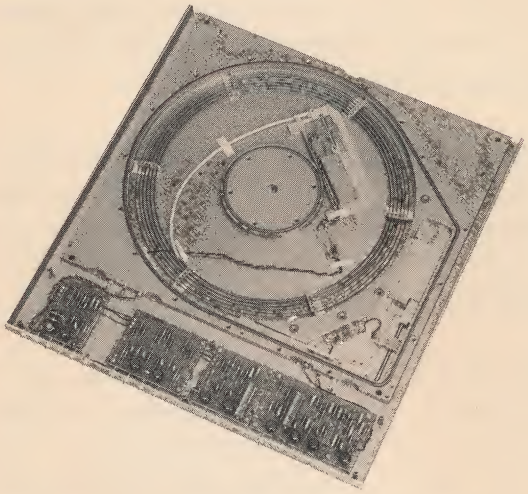
Interface Electronics for Magnetostrictive Delay Line Systems

Magnetostrictive delay lines are ideally suited as storage devices for digital data processing systems. With appropriate electronics they can be made to operate in exact synchronism with any stable clock at bit rates up to 2 mc and higher.

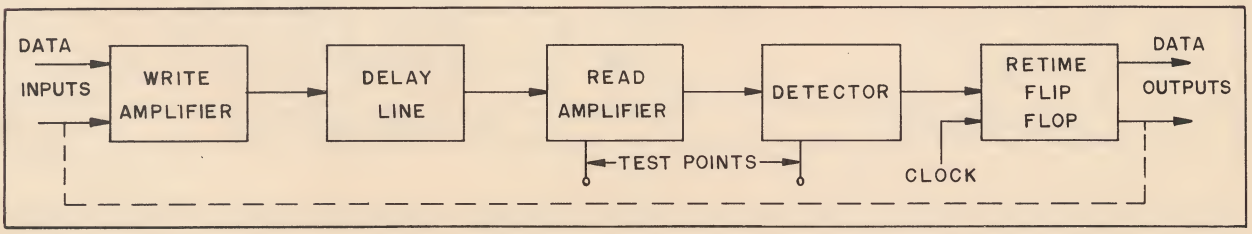


Typical DDI delay line buffer system offers 2000-bit capacity

In any delay line storage, buffer or memory system (these three terms are often used interchangeably) there are four basic types of electronic circuits: 1) the Write (or record) Amplifier; 2) the Read (or playback) Amplifier; 3) the Detector; and 4) the re-timing circuit. Their names convey their functions, as illustrated in the simplified block diagram shown below.

Typically, the write amplifier contains a two-input NOR gate to accept logic levels or pulses from external sources or from the delayed output of the system for recirculation. The write amplifier features high input impedance to minimize loading on external circuitry. Its output impedance is adjusted to match the impedance of the delay line input transducer.

The read amplifier applies linear amplification to the low-level signal induced in the output transducer, raising signal levels to several volts for driving the detector. Detectors vary depending on the mode of recording used. Details of



Block diagram of delay line memory system using DDI interface electronics

the various recording modes and their detection techniques are contained in another DDI Application Note.

The re-timing circuit compensates for any timing variations that occur during the system delay, placing information back in exact synchronism with the system clock -- usually a crystal-controlled source of high stability.

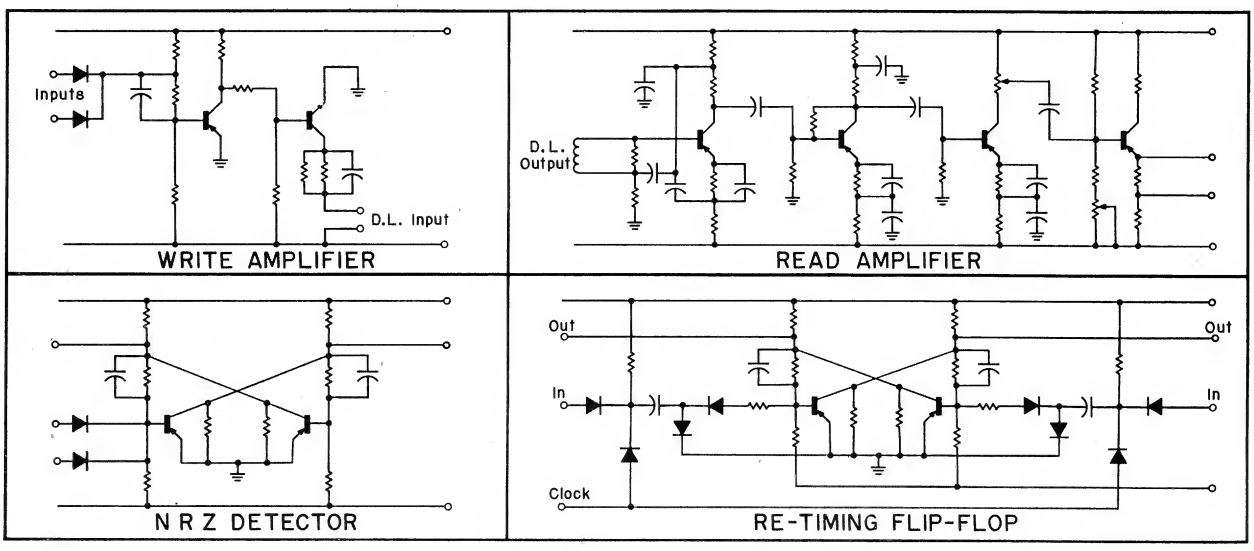
Digital Devices Circuit Modules

Digital Devices, Inc. offers a complete line of modules designed specifically for use with high-performance magnetostrictive delay lines. Through the use of off-the-shelf circuits, a wide variety of systems may be fabricated quickly and inexpensively.

Schematic diagrams of typical standard circuits are shown below. Input and output logic levels are 0 volts $\pm$ 0.5 volt and -4 volts to -15 volts (positive voltages are accomodated with npn transistors in identical circuits). Experienced circuit designers will notice the use of techniques that minimize effects of component aging and power supply fluctuations on circuit performance.

Circuits of the type shown may be purchased from DDI as individual units or in completely integrated systems designed by DDI engineers to do specific functions to customer specifications. Typical of such systems are digital data buffers for tape formatting and communications applications, digital and analog time compression and expansion systems, correlators and many more.

DDI packages are available in commercial and full MIL spec packages, including systems for air and missile-borne applications.



Typical interface electronics circuits for use with magnetostrictive delay lines

Application Note No. 3

DIGITAL DEVICES INC.
WALNUT 1-2400
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Storage Limitations of Clocked Magnetostrictive Delay Line Loops

The delay time of each reclocked module in a serial memory may be temperature or frequency-limited and, for maximum capacity at lowest cost, should be chosen to take simultaneous advantage of both characteristics.

Figure 1 illustrates the maximum attainable bit rates for the three major recording modes in each of three standard-sized packages. A comparison between curves shows that large package size is consistent with maximum utilization of material bandwidth for large amounts of storage. Pulse distortion, primarily low-frequency dispersion, affects NRZ most seriously and eventually (at long delays - see dotted portion of curve) causes detection of information to become unreliable. Phase reversal operation, through use of a clock-energized polarity gate, is least affected.

Controlled-temperature operation is seen to have no effective storage limit (at least for Phase Reversal operation) in the range considered. An upper limit of storage occurs at approximately 20,000 bits where insertion loss (which increases at 2 db/msec in large packages) causes drive power and amplification requirements to become unreasonably severe.

Temperature limitations on delay line length stem from a delay drift characteristic which is proportional to delay length, independent of package size, and is a parabolic function of temperature. A typical Δ delay vs. temperature

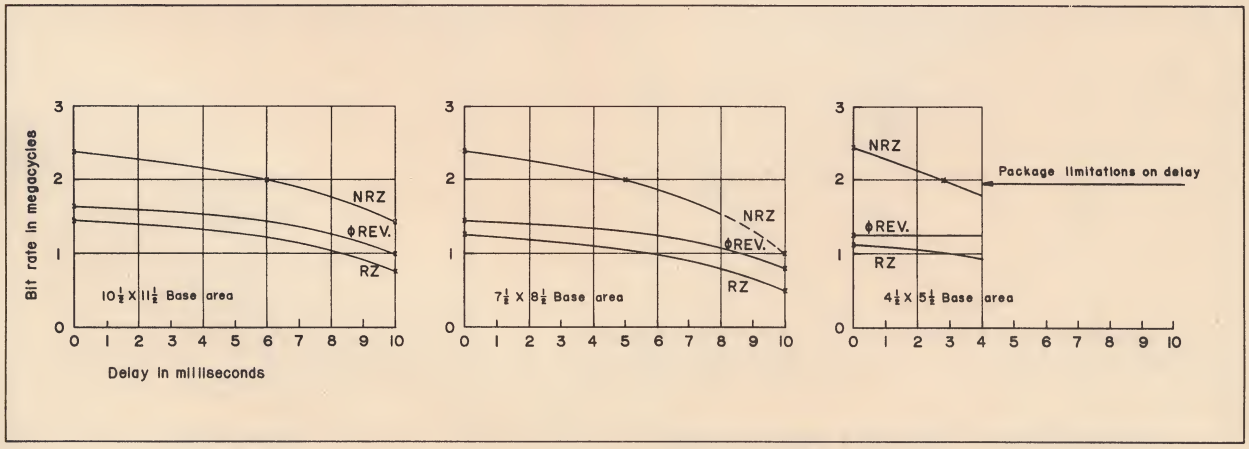

Fig. 1 - Maximum Attainable Bit Rates for Standard DDI Delay Lines

characteristic (for a 3000-microsecond delay line) is shown in Figure 2. The temperature scale is shown as a "deviation from center" rather than an absolute scale because the "center" of the curve may be placed anywhere in the range of -40° to $+ 80^{\circ}C$ by proper preparation of material.

The period available for reclocking of delayed information is proportional to bit rate. Factors which must be taken into account in an analysis of the time available for temperature drift include (a) variation of crystal clock frequency with temperature; (b) temperature-variable phase shift in the read amplifier, (c) trigger variations due to hysteresis in detector circuitry, (d) variations in trigger level (causing shifts in delay since the delay line output waveform has a finite rise time) and, (e) pattern sensitivity in the delay line. The last factor is presumed to be small on the basis that the delay line has sufficient bandwidth for the requirement. Figure 3 shows effects of phase dispersion.

Assessment of currently available circuitry and delay lines has shown that an effective production limit of 10,000 bits may be achieved for a temperature range of $40^{\circ}C$ with a delay line 5000 microseconds long operating at 2 mc/s. The delay variation obtained is typically $\pm$ 0.1 microseconds and properly designed circuitry has kept all other shifts down to .100 microseconds. Larger amounts of storage in a serial memory may be obtained by cascading modules of 10,000 bits each with reclocking performed after each module; there being no limit to this process.

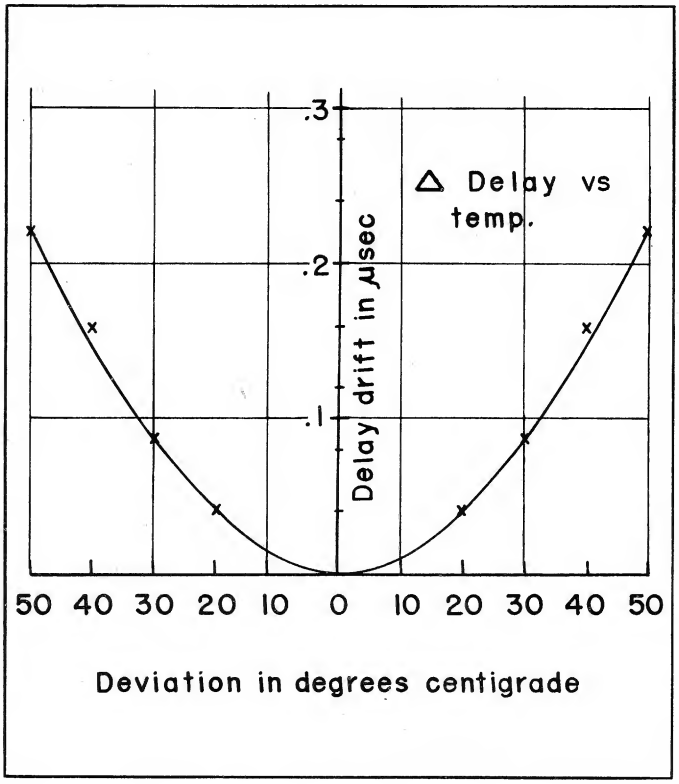

Fig. 2 - Typical Delay vs. Temperature Curve

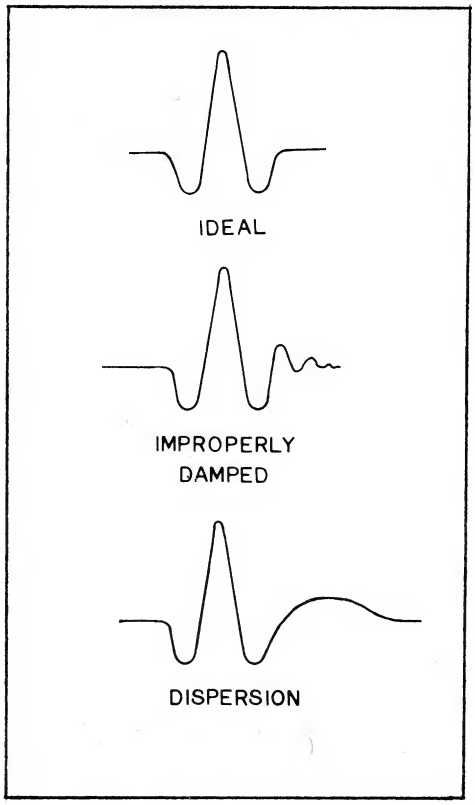

Fig. 3 - Waveforms Showing Effects of Dispersion

Application Note No. 4

(516) WALNUT 1-2400

DIGITAL DEVICES INC.

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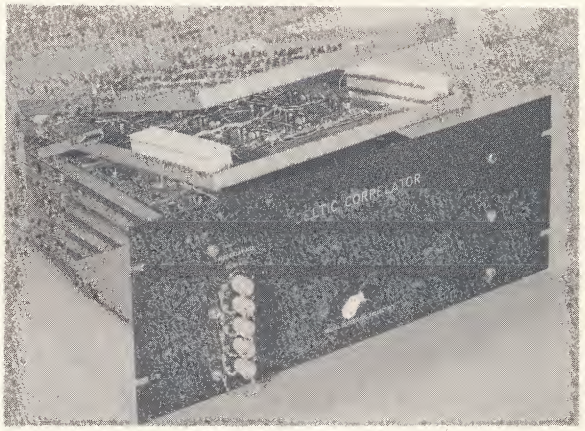
Delay Line Time Compressor



Delay lines can be used to improve signal-to-noise ratios for real-time information processing techniques such as cross-correlation and auto-correlation and spectrum analysis. In such applications, small "bites" or samples of repetitive low frequency signals are taken and stored in the delay line or lines. When a complete cycle of the incoming signal has been thus assembled, the continuously recirculating content of the delay line represents a "squeezed" or compressed replica of the longer period incoming signal -- thus the term DElay Line TIme Compressor, or DELTIC.

As a practical example, consider an incoming signal with a 1 second period that is to be compressed to 1 millisecond. For this purpose a 1 msec delay line is used. The line might typically be divided into 1,000 segments of 1 usec each. At the beginning of the incoming signal cycle, a sample is made and the result stored in the first available storage "cell" of the delay line. Sampling is then interrupted as the stored information travels down the line and finally reaches the recirculation electronics where it is reconstituted and placed back into the line for recirculation.

Immediately after the passage of the last sample, the incoming signal is again sampled (1 msec plus 1 usec later) and the result stored in the next "cell" and so on. After 1,000 recirculations of the line (1 msec times 1,000, or 1 sec) the entire cycle of the incoming signal has been squeezed into the 1 msec line and a condensed version of it is continuously available at a 1-kc rate. Thus the duration of the incoming sample has been reduced by a factor of 1,000 and the frequency components of the signal have been increased by the same factor.

In cross correlation, the compressed signal can then be compared with similarly compressed reference information with discrete changes in relative phase for each recirculation. A complete correlation may be plotted during the time required for a single cycle of the incoming signal. In spectrum analysis, comparison of the compressed signal is performed with respect to variations in frequency.

In high-speed auto-correlation, where the incoming signal is compared with delayed replicas of the same signal, deltics again prove their usefulness by

providing means for storing both signals and, through the use of precession (introducing a small fixed delay in the recirculation loop of the reference line) to provide the necessary timing for the process.

Delay lines may be used in series to increase compressed signal time or in parallel to increase sample resolution. Single lines can provide delays of up to 15 msec. With shorter lines, sample rates of 1 mc are practical. A 10-msec line operating at a 1 mc rate would thus store 10,000 1-usec samples.

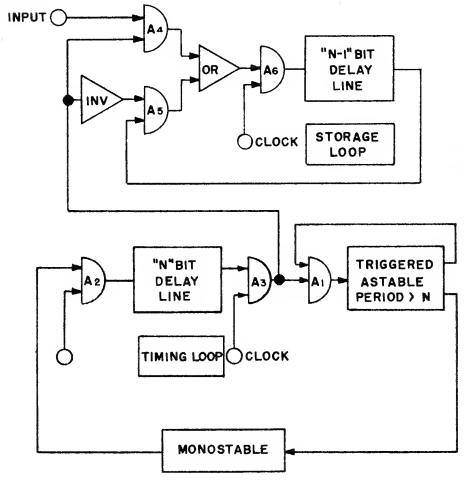
A typical "one bit" delay line time compressor is diagrammed in Fig. 1. Two lines are used, one for storage and one for timing. The first sample is gated into the storage line via A_4 and A_6. When the stored data reaches the end of the storage line, it is amplified and returned to the input of the line via A_5 (which is enabled due to the inverter) and A_6. During the following cell time the timing gate pulse appears at the output of A_3, enabling input gate A_4 and disabling recirculation gate A_5 (interrupting old data during that cell time.) Once filled, the output of the storage loop is a continuous, repetitive, accelerated version of the most recent cycles of the input waveform. Figure 2 shows a block diagram of a cross correlator using delay lines for time compression and timing.

Delay lines can similarly be used as time expanders by sampling a high-frequency phenomenon at the lines basic sampling range and feeding the samples out at the line's recirculation rate, thus achieving a slowdown in the ratio of the line length to the storage cell time.

In the previous examples "one bit" information has been assumed. For greater resolution signals are normally digitized to the required resolution and accuracy. The resulting digital numbers may be entered serially into the line reducing the capacity and rate of the line) or a number of lines may be used in parallel and the digital information applied to the system broadside at the basic sampling rate.

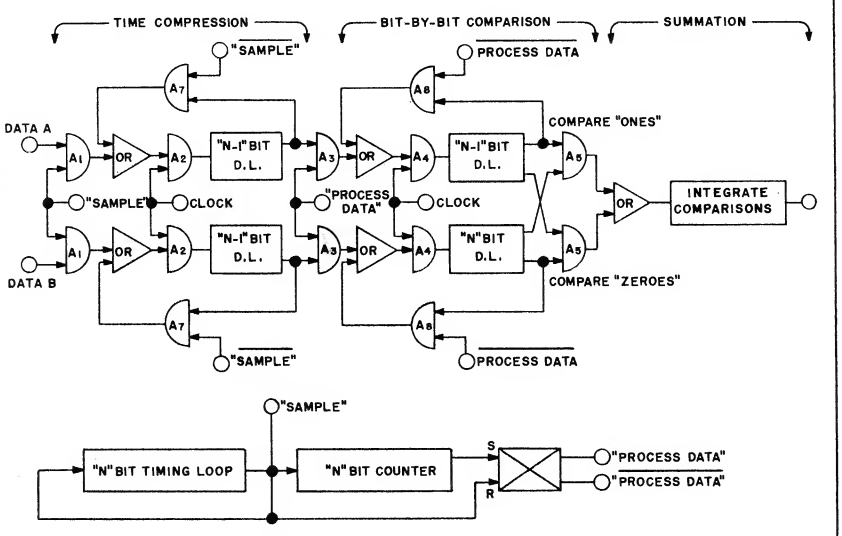
DELTIC

FIG. 1



DELTIC CROSS-CORRELATOR

FIG. 2



Application Note No. 5

DIGITAL DEVICES INC.

WALNUT 1-2400

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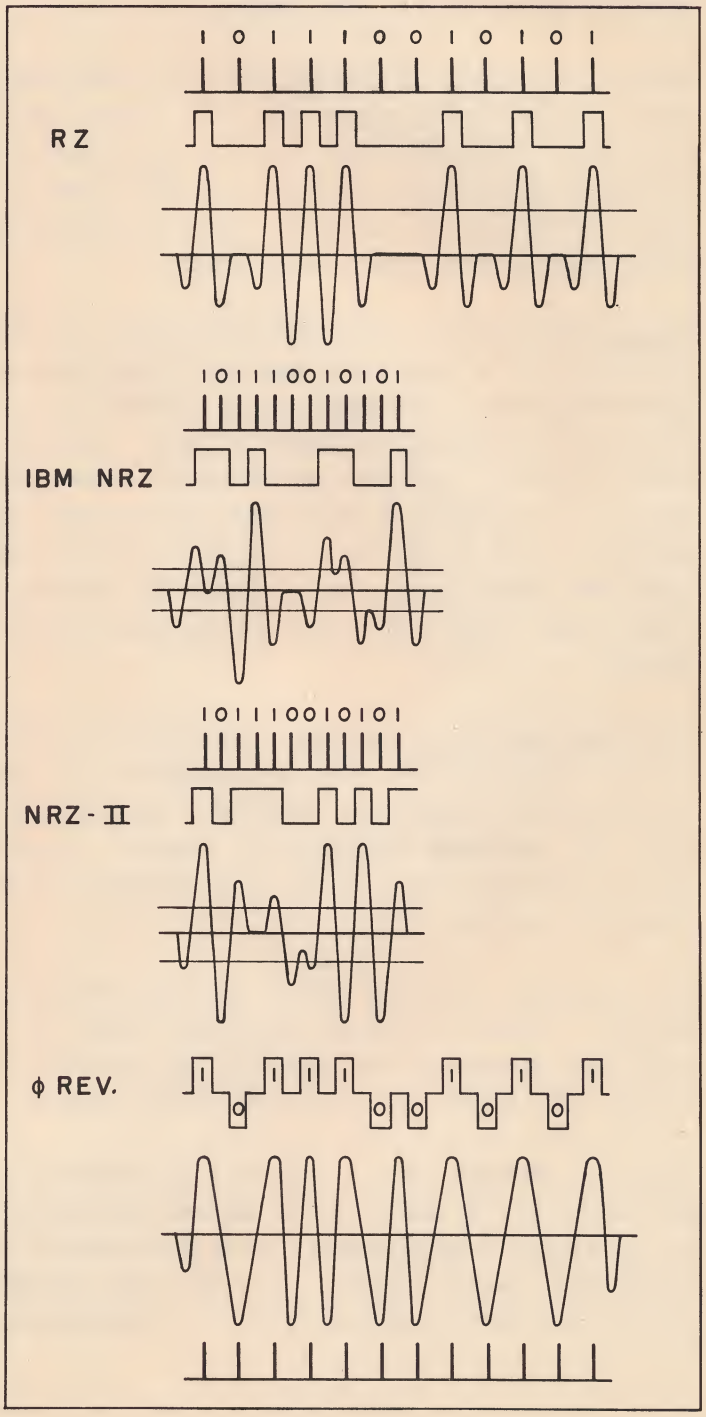
Recording Modes for Magnetostrictive Delay Line Memories

Most magnetostrictive delay line systems employ one of four recording modes. These are illustrated at right and discussed below.



RZ or PULSE Recording uses presence of a pulse to indicate a logic 1 and absence for a "0". Information is recovered by triggering a one-shot at some level above the baseline. Operating bit rate limitations are based on the "triplet" response, typically 1 microsecond for delay lines up to 5 milliseconds in length, for 1 megacycle operation. Signal to noise ratios of 10 to 1 are achievable with this mode, but amplitude variations over wide temperature ranges preclude its use with delay lines longer than 10 milliseconds.

IBM NRZ Recording utilizes the edge response of a delay line to denote a logic 1. Input information changes polarity for each "1" and remains in its previous state for a "0". Triggering a flip-flop on and off at the two levels shown reconstitutes the input code. A 2:1 speed advantage occurs through use of this recording mode, since a bit of information is represented by a single change of state (instead of the two changes required for RZ recording). Noise margins

are half those exhibited by the RZ mode since noise associated with a triplet produced by a double "1" pattern) must be compared against the lower amplitude of the edge-response doublet. Detection at two sensing levels instead of one requires the use of more carefully designed circuitry, as a tradeoff for the higher bit rates achievable (generally in excess of 2 mc).

NRZ Recording, or Level Logic Recording, may be used without code conversion at the input. The edge-response doublet produced by the delay line is utilized in the same way as the IBM NRZ system and a two-level flip-flop reconstitutes the input code. Operating margins are identical to the IBM NRZ system as is the 2:1 advantage in bit rates.

Direct recording of frequency-modulated data may be accomplished through the use of this mode since all information is carried by the location of the zero crossing. Such FM data may be amplified and clipped symmetrically and introduced to the delay line as an NRZ code. The identical pattern is recovered after detection and filtering may be employed, if necessary, to bring the output data back to the exact input form.

Phase Reversal or Bi-Polar Recording is similar to RZ except that a logic 0 is recorded as a pulse of polarity opposite to that recorded for a logic 1. The level detection schemes required for the modes described above is replaced by a clock-synchronized polarity gate, greatly increasing operating levels. This mode exhibits distinct advantages when delay lines are to be operated under substantial shock or vibration conditions, or when wide temperature variations interfere with level detection techniques. Bit rates are limited to a 20-percent increase over those achievable with conventional RZ (and are thus considerably lower than NRZ) but error-free performance can be obtained in hostile environments.

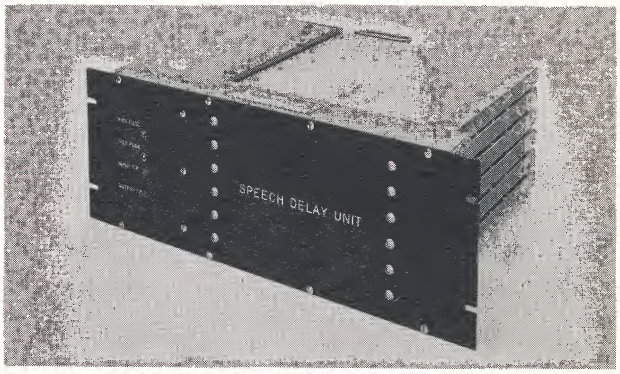
Summary and Conclusions. Comparison of the four modes yields these guidelines: Either of the NRZ techniques will yield maximum operating speed and consequently maximum storage, provided that detection can be accomplished over the required temperature range. A single delay line can provide 10,000 bits of storage for a 40°C temperature range where shock-induced noise is not likely to occur.

RZ recording provides twice the environmental tolerance of NRZ, but at half the speed. Phase reversal recovers some of the speed advantage and provides maximum performance margins for systems required to operate over temperature ranges of -55°C to +125°C or during shocks exceeding 200 g.

Digital Devices, Inc., offers a complete line of interface electronics modules for operating in each of the above mentioned modes. Components are arranged to facilitate modifications to accommodate variations. Customers may specify input and output codes, bit rates and operating conditions and DDI engineers will recommend optimum interface electronics.

MODEL 607E 1000

ANALOG DELAY SYSTEM



The DDI Analog Delay System combines analog and digital techniques to impose precise time delays on analog information using digital magnetostrictive delay lines as the delay medium. Typical applications include sonar data processing, speech and analog data transmission and autocorrelation.

Typical Analog Delay System illustrated delays speech information 60 milliseconds using six 10-msec delay lines with less than 5 percent total signal distortion.

FEATURES

Wide Band — Response within ± 1 db 20 HZ to 20 KHZ
Low Noise — - 50 dbm quiescent
Low Distortion — Less than 5%
High Reliability — No moving parts; nothing to wear out.
Expandable — Delays to over 100 ms by adding sections with up to 10 ms delay each.
Multiple Output — Outputs may be provided after each delay section.

BLOCK DIAGRAM

ELECTRICAL CHARACTERISTICS

Delay Range — 100 usec to over 100 ms
Frequency Response — ± 1 db, 20 HZ to 20 KHZ
Interface Impedance — 600 ohms, balanced or unbalanced
Dynamic Range — 0 dbm to - 40 dbm
Input Signal — 0 dbm max
Output Signal — 0 dbm max
Distortion — 5% max
Noise (quiescent) — - 50 dbm
Power — ± 12 v

MECHANICAL CHARACTERISTICS

Mounting — Rack mountable in a 19" relay rack
Signal Connector — UHF type
Outline Drawing — Per DDI# 607E-1000-000

EXTENDED STORAGE

In applications requiring longer delays of relatively short intervals or bursts of analog information, special techniques are available. A single line, longer than the duration of the data of interest and some submultiple of the desired delay is used. The data is recirculated the required number of times before being transformed back into analog form.

By controlling the number or recirculations a wide range of accurate delays may be obtained. A number of other special techniques are available to help solve other analog data time displacement problems.

MULTIPLE OUTPUTS

As shown in the block diagram, many delay lines are cascaded to provide the total delay required. Output demodulators can tap the delayed signal between any two delay lines, providing multiple output or switch-controlled delay variability.

THEORY OF OPERATION

A magnetostrictive delay line can be considered to be a black box device which delivers a doubly-differentiated replica of its input signal, and introduces a well-controlled amount of delay into this signal. Its bandpass characteristics are linear over a frequency band equal in width to the center frequency of operation. Thus, for a delay line designed to operate at 1.0 MHz, a 3-db bandpass will extend from 0.5 MHz to 1.5 MHz.

Signals in the frequency range of 200 KHz to 4 MHz (the range of center-frequencies to which magnetostrictive delay lines can be designed) will therefore be delayed with essentially constant phase characteristics over their passband, and double-differentiated. In the case of essentially sinusodial data, the output can be considered to be a replica of the input, delayed in time.

In order to delay analog information, this information must therefore be relocated in the frequency spectrum of delay line operation (in this case, approximately 600 KHz because of the line lengths employed) by any suitable modulation technique. FM is the modulation scheme most conducive to low noise operation.

The block diagram illustrates the basic system concept. Delay line modules, of up to ten milliseconds each, are cascaded to make up the required delay. These units pass the supplied FM information without reconversion between delay lines, and final demodulation is accomplished at the system output. At the FM frequencies, the small perturbations introduced in the FM data by the delay lines are minimal with respect to their effect on the original analog data, and many such delay modules may therefore be cascaded without significantly increasing the distortion of the analog data.

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